APPLICATION FOR UNITED STATES LETTERS PATENT
UNITED STATES PATENT AND TRADEMARK OFFICE
(MBHB 00732)

Title: Apparatus and Method for Improving Resolution of a Current Mode Driver

Inventors: Pak Shing Chau, Carl Werner

Attorneys: Denis A Berntsen
Matthew J. Sampson
McDonnell Boehnen Hulbert & Berghoff
300 South Wacker Drive
Chicago, Illinois 60606
312/913-0001

Assignee: Rambus Inc.
2465 Latham Street
Mountain View, CA 94040

Apparatus and Method for Improving Resolution of a Current Mode Driver

CROSS REFERENCE TO RELATED APPLICATION(S)

This application is a continuation-in-part of U.S. Patent Application Serial No.09/655,010, entitled "Method and Apparatus for Calibrating a Multi-Level Current Mode Driver," filed September 5, 2000 which is a continuation-in-part of U.S. Patent Application Serial No. 09/478,916, entitled "Low Latency Multi-Level Communication Interface," filed on January 6, 2000, which claims priority to U.S. Provisional Patent Application Serial No. 60/158,189, entitled "A Method and Apparatus for Receiving High Speed Signals with Low Latency," filed on October 19, 1999, the contents of each of which are incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates generally to the field of electrical buses. More particularly, the present invention relates to a current mode driver for a high speed bus.

BACKGROUND OF THE INVENTION

Computer systems and other electronic systems typically use buses for interconnecting integrated circuit components so that the components may communicate with one another. The buses frequently connect a master, such as a microprocessor or controller, to slaves, such as memories and bus transceivers. Generally, a master may send data to and receive data from one or more slaves. A slave may send data to and receive data from a master, but not another slave.

Each master and slave coupled to a prior bus typically includes output driver circuitry for driving signals onto the bus. Some prior bus systems have output drivers

that use transistor-transistor logic ("TTL") circuitry. Other prior bus systems have output drivers that include emitter-coupled logic ("ECL") circuitry. Other output drivers use complementary metal-oxide-semiconductor ("CMOS") circuitry or N-channel metal-oxide-semiconductor ("NMOS") circuitry.

While many prior buses were driven by voltage level signals, it has become advantageous to provide buses that are driven by a current mode output driver. A benefit associated with a current mode driver is a reduction of peak switching current. In particular, the current mode driver draws a known current regardless of load and operating conditions. A further benefit is that the current mode driver typically supresses noise coupled from power and ground supplies.

A known current mode driver is shown in U.S. Patent No. 5,254,883 (the "'883 patent"), which is assigned to the assignee of the present invention and incorporated herein by reference. The '883 patent discusses an apparatus and method for setting and maintaining the operating current of a current mode driver. The driver in the '883 patent includes an output transistor array, output logic circuitry coupled to the transistor array and a current controller coupled to the output logic circuitry.

For one embodiment, the current controller in the '883 patent is a resistor reference current controller. The current controller receives two input voltages, v_{TERM} and v_{REF}, the latter of which is applied to an input of a comparator. V_{TERM} is coupled by a resistor to a node, which is in turn coupled to a second input of the comparator. The voltage at the node is controlled by a transistor array, which is in turn controlled in accordance with an output of the comparator.

When the transistor array is placed in the "off" state, i.e. there is no current flowing through the transistors of the array to ground, the voltage at the node is equal to v_{TERM}. In addition, by using the output of the comparator to adjustably activate the transistor array, the '883 patent shows that the voltage at the node may be driven to be approximately equal to the reference voltage, v_{REF}.

Knowing the value of v_{REF} and v_{TERM}, the current mode driver of the '883 patent therefore provides a binary signaling scheme utilizing a symmetrical voltage swing about v_{REF}. Specifically, in a first current state (the "off" state), the current mode driver is not sinking current and the signal line (or bus line) is at a voltage, $v_o = v_{TERM}$, representing a logical "0." In a second current state (the "on" state), the current mode driver is sinking current to drive the voltage on the signal line (or bus line) to be:

$$V_o = V_{TERM} - 2\,(V_{TERM} - V_{REF}).$$

The second state therefore representing a logical "1."

While the above techniques have met with substantial success, end users of data processing systems, such as computers, continue to demand increased throughput. Whether throughput is expressed in terms of bandwidth, processing speed or any other measure, the bottom line is the desire to get a block of data from point A to point B faster. At the same time, however, it is desirable to achieve such increases without requiring deviation from known semiconductor fabrication techniques.

SUMMARY OF THE INVENTION

In accordance with a first aspect of the present invention, a method for improving resolution of a current mode driver is provided. The current mode driver is operable to provide an output that falls within a predetermined range. The method includes sensing a condition, such as a process condition, a voltage condition and a temperature condition. A full scale current of a digital-to-analog converter is adjusted in accordance with the condition. A current control signal is set based on an output of the digital-to-analog converter.

In one embodiment, the sensing step includes measuring a process, voltage or temperature sensitive DC parameter. In an alternative embodiment, the sensing step includes sensing a process, voltage or temperature sensitive AC parameter.

In accordance with a second aspect of the present invention, a circuit is provided for improving resolution of a current mode driver. A process-voltage-temperature detector is coupled to the current mode driver. The detector includes circuitry for detecting a process condition, a voltage condition, a temperature condition or any combination of the foregoing. The detector further includes circuitry for providing an output indicative of the detected condition(s). The output of the detector may be used to adjust the current mode driver.

In accordance with a third aspect of the present invention, a digital-to-analog converter is provided for improving resolution of a current mode driver. The digital-to-analog converter provides an analog output in response to a digital input. The output is coupled to one or more transistor gates to control a current mode driver. In one embodiment, the digital input represents at least one of a process condition, a voltage

condition and a temperature condition. In an alternative embodiment, the digital input is set by a register during current control calibration.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a memory controller, bus and memories utilizing an output driver in accordance with a preferred embodiment of the present invention.

Figure 2 illustrates a preferred encoding scheme utilizing a multi-level voltage reference for use with a multi-level output driver.

Figures 3A and 3B are schematic diagrams of a first and a second multi-level output driver in accordance with embodiments of the present invention.

Figure 4A is a graph showing g_{ds} distortion in a transistor.

Figures 4B and 4C illustrate the effect of g_{ds} distortion on the output voltage of a four-level output driver encoding in binary and gray code, respectively.

Figure 5A is an electrical schematic of a multi-level output driver, having a binary generator, that corrects for g_{ds} distortion.

Figure 5B is an electrical schematic of an alternate embodiment of the binary generator shown in Figure 5A.

Figure 6 is an electrical schematic of a circuit to reduce switching noise at an output pin.

Figure 7 is an electrical schematic of a multi-level driver, such as the driver shown in Figure 5A, that further incorporates a circuit to reduce switching noise, such as the circuit shown in Figure 6.

Figure 8 is an electrical schematic of another alternative g_{ds} compensated, multi-level output driver.

Figure 9A is an electrical schematic of a g_{ds} compensated, multi-level output driver with current control circuitry.

Figure 9B is an electrical schematic of a set of stacked transistor pairs for a current drive block, such as the current drive blocks shown in Figure 9A.

Figure 9C is an electrical schematic of a preferred g_{ds} compensated, multi-level output driver.

Figure 10 is an electrical schematic of a circuit for calibrating a g_{ds} compensated output driver with current control circuitry.

Figures 11A and 11B are a flowchart of a method for calibrating the current control circuitry using the setup of Figure 10 for the output driver shown in Figure 9A.

Figure 12 is an electrical schematic of an on-chip, multi-level reference voltage generator utilizing a resistive voltage divider.

Figures 13A and 13B are electrical schematics of a first preferred alternative to the current control calibration circuit of Figure 10.

Figure 13C is a timing diagram for the circuits of Figures 13A and 13B.

Figure 13D illustrates alternative embodiments for the differential comparator of Figure 13B.

Figure 13E illustrates an electrical schematic of a charge coupled comparator using PMOS capacitors.

Figures 14A and 14B are electrical schematics of a second preferred alternative to the current control calibration circuit of Figure 10.

Figures 14C and 14D are timing diagrams for the circuits of Figures 14A and 14B.

Figure 15A is an electrical schematic of a linear transconductor.

Figure 15B is a schematic of a comparator using a transconductor stage.

Figure 16 illustrates output current as a function of the current control bit count for three sets of conditions: slow, typical and fast.

Figure 17 is an electrical schematic of an output driver in accordance with a preferred embodiment.

Figure 18 is an electrical schematic of a first preferred embodiment of a PVT detector.

Figure 19A is a schematic diagram of a second preferred embodiment of a PVT detector.

Figures 19B and 19C are timing diagrams depicting the state of several signals shown in Figure 19A for "slow" conditions and "fast" conditions, respectively.

Figure 20A is an electrical schematic of an embodiment of the PVT detector shown in Figure 19A.

Figure 20B is an electrical schematic of an embodiment of a trigger circuit for the PVT detector shown in Figure 20A

Figure 20C is an electrical schematic of an embodiment of a delay circuit for the PVT detector shown in Figure 20A.

Figure 20D is an electrical schematic of an embodiment of a code generating circuit for the PVT detector shown in Figure 20A.

Figure 20E is an electrical schematic of an embodiment of a decoder circuit for the PVT detector shown in Figure 20A.

Figure 21A is a schematic diagram of a circuit for controlling an output voltage, Vout.

Figure 21B illustrates, for an inverter, the relationship between the input voltage, Vin, and the output voltage, Vout, as a function of the control input, Vg.

Figure 22 is an electrical schematic of a first embodiment of a digital-to-analog converter.

Figure 23 is an electrical schematic of a second embodiment of the digital-to-analog converter.

Figures 24A and 24B illustrate an electrical schematic of a preferred digital-to-analog converter and a simulated output of the digital-to-analog converter, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

In Figure 1, a bus 320 interconnects a memory controller 321 and memories 322. The bus 302 is formed of signal lines 320-1, 320-2 that transmit address, data and control signals. Physically, on each integrated circuit 321, 322, the address, data and control signals are supplied to and output from external connections, called pins, and the bus 320 interconnects respective pins. The bus 320 may be implemented as traces on a printed circuit board, wires or cables and connectors. Each of these integrated circuits 321, 322 has bus output driver circuits 323 that connect to the pins to interface with the bus 320 to transmit signals to other ones of the integrated circuits. In particular, the bus output drivers 323 in the memory controller 321 and in the memories 322 transmit data over the bus 320. Each bus output driver 323 drives a signal line of the bus 320. For example, bus output driver 323-1 in the memory controller 321 drives bus line 320-1. The bus 320 supports signaling with characteristics that are a function of many factors such as the system clock speed, the bus length, the amount of current that the output drivers can drive, the supply voltages, the spacing and width of the wires or traces making up the bus 320, the physical layout of the bus itself and the resistance of a terminating resistor Zo attached to each bus.

At least a subset of the signal lines connect to pull-up resistors Zo that connect to a termination voltage V_{TERM}. In some systems, all signal lines connect to pull-up resistors Zo that connect to the termination voltage V_{TERM}. The termination voltage V_{TERM} can be different from the supply voltage V_{DD}. In one embodiment, the supply voltage V_{DD} is equal to 2.5 volts, the termination voltage V_{TERM} is equal to 1.8 volts, the

bus voltage for a signal at low levels VOL is equal to 1.0 volts, and the voltage swing is 0.8 volts. The resistance of the terminating resistors Zo is equal to twenty-eight ohms.

The output drivers 323 are designed to drive the bus 320 with a predetermined amount of current; and the bus receivers 324 are designed to receive the signals sent by the bus drivers 323 on the bus 320. In a device, each bus receiver 324 receives signals from one signal line of the bus 320. The bus receivers 324 are integrating receivers according to the present invention.

In one embodiment, the memories are random access memories (RAMs). In an alternative embodiment, the memories are read-only memories (ROMs). Alternatively, the bus output drivers 323 and bus receivers 324 of the present invention are implemented in other semiconductor devices that use a bus to interconnect various types of integrated circuits such as microprocessors and disk controllers.

In yet another alternative embodiment, the output drivers are implemented in a point-to-point system. Although a bus that uses current mode signaling has been described with respect to Figure 1, the apparatus and method of the present invention may be used in any signaling system where it is desirable to distinguish between signals having different voltage levels.

Multi-Level Signaling

Referring back to Figure 1, in previously known implementations of the bus system, signals transmitted on each signal line of the bus have either of two voltage levels representing a binary zero or one for binary digital communication. For example, an output voltage equal to the voltage level VTERM set by the voltage source at one end of the termination resistor Zo may represent a binary zero. And, an output voltage level

equal to VTERM – (I*Zo) may represent a binary one, where the output driver circuit 323 sinks an amount of current equal to I. In this way, the bus driver circuits 323 can be implemented as switched current sources that sink current when driving binary one's onto the signal lines. When receiving data, the receiver circuits 324 detect whether the voltage on the signal line is greater than or less than VTERM – 0.5(I*Zo), i.e. the midpoint between a logical zero and a logical one, to determine whether the data is a binary zero or one, respectively. In one embodiment, data is transmitted and received on each edge of the system clock to achieve a data rate equal to twice the frequency of the system clock. In an alternative embodiment, data is transmitted once per clock cycle of the system clock.

As used herein, the term multi-level signaling refers to signaling schemes utilizing two or more signal levels. Multi-level signaling may also be referred to herein as multiple level pulse amplitude modulation, or multi-PAM, signaling, because the preferred coding methods are based upon the amplitude of the voltage signal. Although the multi-level signaling of the preferred embodiments will be described with respect to a current mode bus, multi-level signaling can also be used with a voltage mode bus.

In various embodiments of the present invention, the data rate on a bus is increased without increasing either the system clock frequency or the number of signal lines. Output drivers generate, and receivers detect, multi-PAM signals that allow multiple (k) bits to be transmitted or received as one of 2^k possible voltages or data symbols at each clock edge or once per clock cycle. For example, one preferred embodiment is a 4-PAM system in which two bits are represented by 2^2 or four voltage levels, or data symbols, and the two bits are transferred at every clock edge by

transferring an appropriate one of the four voltage levels. Therefore, the data rate of a 4-PAM system is twice that of a binary or 2-PAM system.

Multi-PAM is not traditionally used in multi-drop bus systems due, at least in part, to the lower signal-to-noise ratio that is realized when the voltage range is divided into multiple levels. Prior art memory systems have been implemented as only binary systems. A preferred embodiment allows such systems to be implemented using more than two signal levels.

In Figure 2, a graph shows one embodiment utilizing a 4-PAM signaling scheme. Specifically, the multi-PAM voltage levels are associated with two-bit binary values or symbols such as 00, 01, 10 and 11. In the embodiment of Figure 2, the binary values are assigned to voltage levels using Gray coding, i.e. the symbol sequence from the highest voltage level to the lowest voltage level is 00, 01, 11, 10. Gray coding provides the advantage of reducing the probability of dual-bit errors because only one of the two bits changes at each transition between voltage levels. If a received 4-PAM voltage symbol is misinterpreted as an adjacent symbol, a single-bit error will occur.

The y-axis of the graph in Figure 2 shows the associated 4-PAM output voltages V_{OUT} for each symbol. To provide the appropriate voltage to transmit a 4-PAM symbol, the output driver sinks a predetermined amount of current for that symbol. In particular, each symbol is associated with different amount of current. To transmit the symbol "00", the output driver 323 sinks no current and the signal line is pulled up to V_{TERM}. To transmit the symbol "01", the bus output driver 323 sinks a predetermined amount of current I 01 to cause the output voltage V_{OUT} to equal $V_{TERM} - 1/3\ (I \cdot Zo)$, where I01 is equal to 1/3 I. To transmit the symbol "11", the bus output driver 323 sinks a

predetermined amount of current I11 to cause the output voltage VOUT to equal VTERM - 2/3 (I · Zo), where I11 is equal to 2/3 I. To transmit the symbol "10", the bus output driver 323 sinks a predetermined amount of current I to cause the output voltage VOUT to equal VTERM -(I · Zo). Further details regarding preferred embodiments of the output driver 323 are provided below.

A 4-PAM receiver identifies a received symbol based on a voltage range or range of voltages associated with that symbol. A set of reference voltages VREFLO, VREFM and VREFHI function as thresholds to define ranges of voltages associated with each 4-PAM symbol. In accordance with a preferred embodiment, the reference voltages VREFLO, VREFM and VREFHI are set at the midpoint voltage between neighboring symbols. For example, the symbol "00" is associated with voltages greater than VREFHI. The symbol "01" is associated with voltages falling within the range between VREFHI and VREFM. The symbol "11" is associated with a range of voltages from VREFM to VREFLO. The symbol "10" is associated with a range of voltages less than VREFL0. The reference voltages VREFHI, VREFM and VREFLO are threshold voltages from which a multi-PAM data symbol is determined to be one of the four possible data symbols.

4-PAM symbols or signals also allow for direct compatibility with 2-PAM or binary signaling. When operating in 4-PAM mode, the received data bits are compared to the three reference voltages, VREFHI, VREFM and VREFLO to determine the 4-PAM symbol and the associated two bits. Because the most significant bit (MSB) is determined by comparing the received data bit to VREFM, i.e.the MSB is zero for voltages greater than VREFM and the MSB is one for voltages less than VREFM, the multi-PAM system can be used as a 2-PAM system by ignoring the least significant bit (LSB) and

using the MSB. Alternatively, to transmit 2-PAM symbols using the gray code of Figure 2, the LSB is set equal to zero (low), while the MSB determines the output voltage.

Multi-PAM signaling increases the data rate with a small increase in power consumption because the number of input/output (I/O) pins and the system clock frequency may be the same as that used for binary signaling. The major factor in the power consumption of CMOS circuits, for example, is the CV^2F power, which depends directly on the system clock frequency. Therefore, increasing the system clock frequency to increase the data rate directly increases the power consumption. Although some additional power is used for the additional circuitry of the multi-PAM interface, described below, this increase in power is much less than the increase in power that would occur if either the number of I/O pins or the system clock frequency were increased to increase the data rate.

Multi-PAM signaling also increases the data rate without a corresponding increase in the electro-magnetic interference (EMI). If the data rate were increased by increasing the number of I/O pins or by increasing frequency, the EMI would increase proportionally. Because multi-PAM signaling does not increase the number of I/O pins, the EMI does not increase if the total voltage amplitude of the multi-PAM I/O pins remains the same as that used in binary signaling. The total voltage amplitude may be increased to provide greater voltage margin to improve system reliability. Although the EMI would increase correspondingly, the increase would be smaller than that incurred by increasing the number of I/O pins with binary signaling.

Although the circuits described below use 4-PAM signaling, the embodiments described can be expanded for use in 8-PAM, 16-PAM and, more generally, N-PAM

signaling. Accordingly, it is to be understood that the preferred embodiments are not limited to 4-PAM signaling, but rather may be applied to the general, N-PAM signaling, case.

In Figure 3A, a 4-PAM output driver circuit 950 is used with current control bits (CCtrl<6:0>) to produce desired output voltage levels over a set of on-chip process, voltage and temperature (PVT) conditions. In the output driver 950, a first driver circuit 952 and a second driver circuit 954 connect to an I/O pin 956. The first driver circuit 952 drives the LSB, while the second driver circuit 954 drives the MSB. The first driver circuit 952 and the second driver circuit 954 have a set of driver blocks 958 that are connected in parallel. Since the driver blocks have the same components, one driver block 958 will be described. Each driver block has a binary weighted driver transistor 960-0 with a width to length (W/L) ratio as shown. The driver transistors 960 of the second driver circuit 954 are preferably twice as large as the driver transistors of the first driver circuit 952 because the second driver circuit 954 drives the MSB while the first driver circuit 952 drives the LSB. In other words, the MSB is driven with twice as much current as the LSB.

In driver block 958, odd and even data bits are multiplexed onto the driver transistors 950 via passgates 962 and an inverter 964. In this embodiment, odd data is transmitted at the rising edge of the clock, while even data is transmitted at the falling edge of the clock. NAND gates 966, 968 connect to current control bit zero <0>, and the LSB Odd Data bit and LSB Even Data bit, respectively. When the respective current control bit zero <0> is high, the NAND gates 966, 968 are responsive to the odd and even data. When the respective control bit is low, the output of the NAND gates 966, 968 is

low and driver block 958 does not respond to the data bit. The current control bits provide the specified amount of current to cause the desired voltage swing regardless of the PVT conditions. The circuit of Fig. 3A uses seven current control bits. Techniques for determining the setting of the current control bits are described below.

The passgates 962 include two transistor pairs, each pair including a PMOS transistor 972, 974 connected in parallel with an NMOS transistor 976, 978. The clock and clock_b signals connect in an opposite manner to the gates of the transistors of the transistor pair.

Although Figure 3A shows that the first driver circuit 952 drives the LSB and the second driver circuit 954 drives the MSB, in an alternative embodiment, the first driver circuit 952 drives the MSB and the second driver circuit 954 drives the LSB. Alternatively, any arbitrary coding scheme can be produced by placing combinational logic to combine the data bits before sending the combined data bit to the driver block 958.

Table 1 below shows two 4-PAM encoding schemes that may be implemented using the output driver 950 of Figure 3A.

Table 1: Encoding Schemes

Coding Scheme	Data Bits (Symbol) to be Transmitted	MSB Input	LSB Input	Output Voltage
Binary	00	0	0	VTERM
	01	0	1	VTERM – 1/3 (I·Zo)
	10	1	0	VTERM – 2/3 (I·Zo)
	11	1	1	VTERM – (I·Zo)
Gray	00	0	0	VTERM
	01	0	1	VTERM – 1/3 (I·Zo)
	11	1	1	VTERM – 2/3 (I·Zo)
	10	1	0	VTERM – (I·Zo)

In another embodiment shown in Figure 3B, a 4-PAM output driver 980 uses current control bits to control switch transistors in series with the output current source transistors, resulting in the desired output voltage levels. Two sets 981-1 and 981-2 of binary weighted transistors 982-986 combine the current control bits with 4-PAM signal generation. The current control bits directly control current-control NMOS transistors 982-2, 984-2, 986-2 that are connected in series with the driver transistors 982-1, 984-1, 986-1, respectively, that receive the LSB and MSB data. For odd data, the driver transistors 982-1, 984-1, 986-1, cause current to flow to the I/O pin 956 when the respective data bit and the clock signal are high, and the associated current control bit is high to place NMOS transistors 982-2, 984-2 and 986-2 in the active state.

The circuit for even data is not shown, but a separate set of current control NMOS transistors connects in series with a set of driver transistors that respond to the logical "AND" of the respective data bit and the complement of the clock signal Clock_b for even data.

The output voltages of the circuits of Figures 3A and 3B include gds distortion from the driver transistors. In Figure 4A, a graph shows gds distortion. The x-axis shows the drain-to-source voltage, and the y-axis shows the drain current. Specifically, gds of a MOS transistor is the change of drain current in response to a change in drain voltage. Figures 4B and 4C show the data bits, in binary and gray code respectively, and the effect of gds distortion on the output voltage VOUT. In particular, as the output voltage VOUT decreases, the incremental voltage difference between adjacent 2-bit pairs decreases. Because of gds distortion, the voltage increments between the 4-PAM voltages are generally not equal.

In Figure 5A, a 4-PAM output driver 1000 that corrects for gds distortion is shown. The output driver 1000 is two-way multiplexed, with the multiplexing occurring at the I/O pin 956. The output driver is of the open-drain type and operated in current-mode, with the output current set by a bias voltage on a current source device coupled in series with each of the transistors 1002, 1004 and 1006. For simplicity the current control transistors are not shown. In accordance with a preferred embodiment, a new output symbol is generated on each rising and falling edge (referred to herein as "odd" and "even," respectively) of the clock.

The gds distortion is eliminated by adjusting the width to length (W/L) ratio of transistors 1004 and 1006 by factors α and β, such that $\beta>\alpha>1$ and the incremental voltage difference between adjacent 4-PAM levels is constant. Transistors 1002, 1004 and 1006 have a width to length ratio of W/L, α(W/L), and β(W/L) respectively.

Examples of encoding schemes that may be implemented using the output driver of Figure 5A are shown in Table 2 below. In accordance with a preferred embodiment, input signals A, B, and C are derived from the MSB and LSB of a symbol to be transmitted to produce the 4-PAM levels as shown in Table 2 below. The encoder of the output driver 1000 uses combinational logic 1007 to produce the A, B and C inputs according to Table 2.

Table 2: Mapping of Data Bits to ABC Inputs and Encoding Schemes

Coding Scheme	Data Bits (Symbol) to be Transmitted	A	B	C	Output Voltage
Binary	00	0	0	0	VTERM
	01	1	0	0	VTERM – 1/3 (I·Zo)
	10	1	1	0	VTERM – 2/3 (I·Zo)
	11	1	1	1	VTERM – (I·Zo)
Gray	00	0	0	0	VTERM
	01	1	0	0	VTERM – 1/3 (I·Zo)
	11	1	1	0	VTERM – 2/3(I·Zo)
	10	1	1	1	VTERM – (I·Zo)

A binary encoder 1007 is illustrated in Figure 5B. In the encoder 1007, an OR gate 1008 generates the A signal by performing an OR operation between the LSB and MSB. The B input is the MSB. An AND gate 1009 generates the C signal by performing an AND operation between the LSB and MSB.

In Figure 5C, an alternative preferred encoder 1007 encodes the LSB and MSB using Gray code. The encoder 1007 of Figure 5C is the same as the encoder 1007 of Figure 5B except that, to generate the C signal, the AND gate 1009a receives the complement of the LSB rather than the LSB.

In Figure 9C, an alternative preferred embodiment of the gds compensated output driver is shown. In this embodiment, the output driver has separate odd and even symbol encoders, with the encoder outputs being multiplexed at the gates of the output transistors.

On-chip, single-ended output drivers, as shown in Figures 3A and 3B generate switching noise. For example, when the transistors in the output driver transition from sinking no current such as when driving the "00" symbol, to sinking maximum current such as when driving the gray-coded "10" symbol, the current surges through the I/O pin 956 and through a ground pin. The path between I/O pin 956 and ground has inherent inductance that opposes the current surge and produces significant switching noise (i.e., ground bounce). Because the voltage margins for multi-PAM signaling are less than the voltage margins for binary signaling, switching noise may cause decoding errors.

To reduce sensitivity to switching noise, output drivers can provide a constant or semi-constant current to ground regardless of the output current being driven. As shown

in Figure 6, each single-ended transistor branch 960 (Figure 3A) and 986 (Figure 3B) in the output drivers of Figures 3A and 3B is replaced with a differential pair 1010.

When the output driver sinks output current from the I/O pin 956, current is steered through transistor N1 1012 to ground. When transistor N1 1012 is inactive, transistor N2 1014 becomes active to allow the same or substantially the same amount of current to flow to ground. In this way, a substantially constant amount of current continuously flows to ground to eliminate a large portion of the output driver switching noise and provide a quieter on-chip ground, thereby improving the performance of the 4-PAM signaling. The signal Vi, is the signal that drives transistor N1 1012. Alternatively, the signal V_R that drives transistor N2 1014 is a reference voltage between ground and Vi. In response to an input voltage V_{Cntrl}, the current source 1016 sinks a predetermined current Io to ground.

Figure 7 is another embodiment of a multi-PAM output driver that combines the circuit of Figure 5A, which eliminates gds distortion, with the circuit of Figure 6 to reduce sensitivity to switching noise.

In Figure 8, yet another gds compensated 4-PAM output driver is shown. In the 4-PAM output driver, the A, B, and C signals drive equal-sized NMOS transistors 1018, 1020, 1022 having width W. In accordance with a preferred embodiment, signals B and C also drive NMOS transistors 1024, 1026 of width W_B and Wc, respectively, to compensate for gds distortion. The widths of the NMOS transistors 1024 and 1026, W_B and Wc, respectively, are chosen such that the difference between output levels for adjacent bits is substantially the same, such as 1/3 (I·Zo). The widths of the transistors 1018-1026 may therefore have the following relationship:

$$W+Wc > W+Wb > W$$

In Figure 9A, a 4-PAM output driver corrects the gds distortion and provides current control. As described above, the signals A, B and C preferably determine the output voltage or symbol in accordance with the gray-coded binary signaling shown in Table 2, above. In addition, three sets of current control calibration bits, CC, CCB and CCC, respectively determine the amount of current supplied by the output driver for various combinations of A, B and C. The first set of control bits CC provides primary current control, while the second and third sets of current control bits, CCB and CCC, respectively, fine tune the amount of current. The first set of current control bits CC has N bits; the second set of current control bits CCB has n1 bits; and the third set of current control bits CCC has n2 bits. In one embodiment, the relationship between the numbers of current control bits is as follows:

$$n1 \leq n2 < N.$$

There may be different relationships between N, n1 and n2 in alternative embodiments.

Each of the A, B and C signals is associated with a current drive block 1040 to drive a predetermined amount of current associated with the symbol. Each current drive block 1040 includes one or more sets of stacked resistor pairs 1042 that are associated with each set of current control bits for that current driver block 1040. For example, the current drive block 1040-1 that drives the A signal receives current control bits CC. The current drive block 1040-2 that drives the B signal receives current control bits CC and CCB. The amount of current supplied by current drive block 1040-2 is adjusted for gds distortion using the CCB bits. The current drive block 1040-3 that drives the C signal

receives current control bits CC and CCC. The amount of current supplied by current drive block 1040-3 is adjusted for gds distortion using the CCC bits.

Referring also to Figure 9B, a set of stacked transistor pairs 1042 is shown. Each stacked transistor pair 1042 includes two NMOS transistors 1046, 1048 connected in series. The lower NMOS transistor 1046 connects to the one of the A, B, or C signals associated with the current drive block 1040. The upper NMOS transistor 1048 connects to a current control bit. The lower NMOS transistor 1046 is preferably wider than the upper NMOS transistor 1048. Because there are N current control bits, there are N stacked transistor pairs. For example, the current control block 1040 has N stacked transistor pairs 1042-1 to 1042-N, and each stacked transistor pair connects to one of the current control bits, CC <0> to CC <N-1>.

The transistors of the stacked transistor pairs are binary weighted with respect to minimum width of W1 for the upper transistors and W2 for the lower transistors. The widths W1 and W2 may be chosen to determine output characteristics such as output resistance and capacitance. Generally the widths W1 and W2 are chosen such that W1 is less than W2.

Although drawn to illustrate the circuit for the CC current control bits, the circuit diagram of Figure 9B also applies to the sets of stacked transistor pairs associated with the CCB and CCC current control bits.

As shown in Figure 10, a current control calibration circuit 1050 determines the settings for the current control bits CC, CCB and CCC by selecting a current control reference voltage, VREF, and comparing the current control reference voltage, VREF, to a voltage at a mid-point between two calibration output voltages, VOUT-1 and VOUT-2.

The current calibration circuit 1050 determines settings for each of the sets of current control bits CC, CCB and CCC for each 4-PAM output voltage such that VOUT-1 and VOUT-2 provide each adjacent pair of voltage levels to the circuit.

A multiplexor 1052 receives the three 4-PAM reference voltages VREFHI, VREFM and VREFLO. A select reference voltage signal, SelRef, selects one of the referenced voltages as the selected current control reference voltage, VREF. A comparator 1054 compares the selected current control reference voltage VREF to a mid-point voltage Vx and generates a comparison signal.

To generate the mid-point Vx, output driver 1 1056 sinks a first amount of current to provide the first output voltage VOUT-1 and output diver 2 1058 sinks a second amount of current to provide the second output voltage VOUT-2. Two passgate pairs 1060, 1062, in response to a current control enable and its complementary signal, act as a resistor divider to provide the midpoint voltage, Vx, between the first output voltage, VOUT-1, and the second output voltage, VOUT-2.

A state machine 1064 includes first, second and third counters, 1066-1, 1066-2 and 1066-3 that provide the first, second and third sets of current control bits, CC, CCB and CCC, respectively. If the comparison signal indicates that the midpoint signal Vx is greater than the reference voltage VREF, the state machine 1064 increments an associated set of current control bits by one to increase the amount of current that is sunk by the output driver, thereby decreasing the midpoint voltage. If the midpoint voltage signal Vx is less than the current control reference voltage, VREF, the state machine 1064 decrements the associated current control bits by one, thereby increasing the midpoint voltage.

In one embodiment, the current control bits are calibrated during a power-up sequence. The theory of operation for calibrating the current control bits is as follows. The first set of current control bits CC provides the primary amount of current control for each current control block 1040. To compensate for gds distortion, the CCB and CCC current control bits fine tune the amount of current associated with the Gray-coded "11" and "10" signals, respectively. The current control bits are preferably calibrated in the following order: CC, CCB, then CCC.

In alternative embodiments, the current control bits may be calibrated after power-up in response to triggering events, e.g., lapse of a period of time, a change in ambient temperature, a change in power supply voltage, or in response to a threshold number of errors.

Referring also to Figure 4B, the first and main set of current control bits CC are set using the voltage differences between the "00" and "01" symbols. The first set of current control bits CC are set to provide a amount of current to provide the output voltage for the "01" symbol such that VREFHI is placed at the midpoint between the output voltage for the "00" symbol and the output voltage for the "01" symbol.

As shown in Figure 4B, because of gds distortion, without compensation, the voltage difference between the "01" symbol and the "11" symbol is less than the voltage difference between the "00" symbol and the "01" symbol. To compensate for the gds distortion, the output voltage for the "11" symbol is decreased by increasing the amount of current sunk by the output driver. The second set of current control bits CCB are set to increase the current sunk by the output driver such that the output voltage becomes equal

to the desired voltage level when the midpoint voltage between output voltage for the "01" and "11" is equal to VREFM.

Finally, the third set of current control bits CCC is adjusted such that the midpoint voltage between output voltage for the "11" and "10" symbols is equal to VREFL.

Referring to Figures 10, 11A and 11B, the operation of the circuit 1050 including the state machine 1064 will be described. The flowchart of Figures 11A and 11B uses gray coded output voltages. In step 1070, the current control enable signal (ccen) and its complement (ccenb) are set to activate the passgate pairs 1060 and 1062 and output the midpoint voltage Vx, described above.

Three major blocks of steps 1072, 1074 and 1076 set the current control bits, CC, CCB and CCC, respectively.

In block 1072, step 1078 sets the initial conditions for determining the settings for the first set of current control bits CC. The state machine 1064 outputs the select reference voltage signal (SelRef), which causes the multiplexor 1054 to output the reference voltage VREFHI to the comparator 1054. A "00" symbol is supplied to output driver 1 1056 by outputting multi-PAM bit selection signals A1, B1 and C1 with values of zero. A "01" symbol is supplied to output driver 2 1058 by outputting multi-PAM bit selection signals A2 with a value of one, and B2 and C2 with a value of zero. The initial state of the first, second and third current control bits is as follows:

$$CC = \{1\ 0\ 0\ \ldots 0\};$$

$$CCB = \{1\ 0\ 0\ \ldots 0\}; \text{ and}$$

$$CCC = \{1\ 0\ 0\ \ldots 0\}.$$

The current control bits are initially set such that the stacked transistor pair sinking the most current will be activated.

In step 1080, the output drivers 1 and 2 output the voltages corresponding to the symbols "00" (the Vterm refernce) and "01" (the drive level under calibration) and the midpoint voltage Vx is generated. In step1082, the comparator 1054 compares the midpoint voltage Vx to the selected reference voltage VREFHI. When the midpoint voltage is within one least significant bit of the reference voltage VREFHI, the first set of current control bits have the proper setting. The state machine 1058 determines that the midpoint voltage Vx is within one least significant bit of the reference voltage VREFHI when the current control bits begin to dither between two settings. In other words, the output of the comparator will alternate between a zero and a one.

In step 1084, when the midpoint voltage Vx is not within one least significant bit of the reference voltage VREFHI, the state machine 1064 augments the first set of current control bits depending on the result of the comparison. The term "augment" is used to indicate either incrementing or decrementing the current control bits. The process proceeds to step 1080.

If, in step 1082, the state machine 1064 determines that the midpoint voltage Vx is within one least significant bit of the reference voltage, the process proceeds to step 1086 to calibrate the second set of current control bits, CCB.

In step 1086, the initial conditions for calibrating the second set of current control bits CCB are set. The state machine 1064 outputs the select reference voltage signal (SelRef), which causes the multiplexor 1054 to output the reference voltage VREFM to the comparator 1054. A "01" symbol is supplied to output driver 1 1056 by outputting multi-

PAM bit selection signals A1 with a value of one, and B1 and C1 with values of zero. A "11" symbol is supplied to output driver 2 1058 by outputting multi-PAM bit selection signals A2 and B2 with a value of one, and C2 with a value of zero. The state of the first set of current control signals CC remains unchanged. The initial state of the second and third sets of current control bits, CCB and CCC, respectively, is as follows:

$$CCB = [\ 1\ 0\ 0\ \ldots\ 0\};$$

$$CCC = [\ 1\ 0\ 0\ \ldots\ 0\}.$$

In step 1088, the output drivers 1 1056 and 2 1058 output the voltages corresponding to the symbols "01" (the level calibrated in step 1072) and "11" (the level now under calibration), and the passgate pairs 1060, 1062 output the midpoint voltage Vx. In step 1090, the comparator 1054 compares the midpoint voltage Vx to the selected reference voltage VREFM. When the midpoint voltage is not within one least significant bit of the reference voltage VREFM, as described above with respect to VREFHI, in step 1092, the state machine 1064 augments the second set of current control bits CCB by one and the process repeats at steps 1086.

When the midpoint voltage is within one least significant bit of the reference voltage VREFM, as described above with respect to VREFHI, the second set of current control bits CCB have the proper setting and the process proceeds to step 1094 to calibrate the third set of current control bits, CCC.

In step 1094, the initial conditions for calibrating the third set of current control bits CCC are set. The state machine 1064 outputs the select reference voltage signal (SelRef), which causes the multiplexor 1054 to output the reference voltage VREFLO to comparator 1054. A "11" symbol (calibrated in step 1074) is supplied to output driver 1

1056 by outputting multi-PAM bit selection signals A1 and B1 with a value of one, and C1 with a value of zero. A "10" symbol (the level now under calibration) is supplied to output driver 2 1058 by outputting multi-PAM bit selection signals A2, B2 and C2 with a value of one. The state of the first and second sets of current control signals CC and CCB, respectively, remains unchanged. The initial state of the third sets of current control bits CCC is as follows:

$$CCC = \{ 1\ 0\ 0 \ldots 0 \}.$$

In step 1096, the output drivers 1 1056 and 2 1058 output the voltages corresponding to the symbols "11" and "10" and the passgate pairs 1060, 1062 output the midpoint voltage Vx. In step 1098, the comparator 1054 compares the midpoint voltage Vx to the selected reference voltage VREFLO. When the midpoint voltage is not within one least significant bit of the reference voltage VREFLO, as described above with respect to VREFHI, in step 1100, the state machine 1064 augments the third set of current control bits CCC by one and the process repeats at step 1094.

In step 1098, when the midpoint voltage is within one least significant bit of the reference voltage VREFLO, the appropriate settings for the first, second and third sets of current control bits, CC, CCB and CCC respectively are determined and the calibration is complete.

For the foregoing embodiment, a sequential search is described: starting at an initial value and augmenting. It should be emphasized, however, that alternative search techniques known to those skilled in the art may be used. For example, without limiting the foregoing, successive approximation using a binary search may be used. As a further,

although less desirable because it is hardware intensive, alternative, a direct flash conversion may be used.

As described above, the current control bits may be augmented until the output of a current control calibration circuit dithers. The resolution of the current mode driver, as that term is used herein, therefore corresponds not only to the number of current control bits that are used but also to the voltage swing that the current mode driver provides. In other words, once the current control calibration circuit locks onto the proper output voltage level, the output voltage level will be dithering within a tolerance range, where the tolerance range is proportional to the minimum current step size of the current control circuit.

It has been observed that certain conditions, including process variation, supply voltage variation and temperature variation, may affect the current that is available from a current mode driver. One approach to compensating for such considerations is to calibrate the output driver so that, at the worst case conditions and with the current control bits set to their maximum, full scale count, the output driver provides at least the minimum required current, Imin. For an embodiment in which each augmentation of the current control bits results in a ratiometric step-size change in current, the current change associated with a change in the least significant bit ("LSB") of the current control bits, LSB(I), may be represented as:

$$LSB(I) = Imin/2^{N}\text{-}1,$$

where N is the number of current control bits. The corresponding voltage, LSB(V), is:

$$LSB(V) = Vmin/2^{N}\text{-}1,$$

where Vmin = Imin * Rterm.

A shortcoming of this approach, however, is that the absolute LSB step size increases as the output driver current capability increases. Figure 16 illustrates output current as a function of the current control bit count for three sets of conditions: slow, typical and fast. As shown, whereas Imin is provided at the full scale count under worst case conditions, i.e. the slow condition (minimum current drive capability), the output current is greater than Imin under the typical and fast conditions, at the same current control bit count. This results in an increase in LSB(I) under the typical and fast conditions, thereby resulting in a corresponding decrease in resolution of the current mode driver under such conditions.

In a multi-PAM system, it is desirable that the current step LSB(I) associated with the LSB of the current control bits be very small in comparison to the change in current between logic levels. Therefore, in accordance with a preferred embodiment of the present invention, a method is provided for improving the resolution of the current mode driver. A preferred method causes the full scale current under typical and fast conditions to be set closer to the full scale current under slow conditions. This not only results in improved resolution by reducing LSB(I) under typical and fast conditions, but also provides the benefit of reducing the variation of LSB(I) as conditions vary.

Figure 17 is an electrical schematic of an output driver in accordance with a preferred embodiment. The output driver includes a reference current source 2000 that is coupled to a current control digital-to-analog converter ("DAC") 2010. The DAC 2010 is also coupled to receive an N-bit current control signal, CC. The DAC 2010 provides an output current, Iout, whose value is dependent upon the current supplied by the reference current source 2000 and the current control signal, CC.

A process-voltage-temperature ("PVT") detector 2020, further described below, provides control signals, S1 and S2, to the reference current source 2000. The control signals S1 and S2 are utilized to adjust the reference current, Iref, supplied by the reference current source 2000 to the DAC 2010 in accordance with the PVT conditions. For example, as illustrated in Figure 17, the control signals S1 and S2 may control switches, such as FET switches, to alter the reference current, Iref, in accordance with:

$$Iref = Ir + S1 \times Ir1 + S2 \times Ir2, \text{ where } S1, S2 = \{0,1\}$$

and,

$$LSB(I) = Iref / 2^{N}-1.$$

As an example of the concern raised by PVT variations, consider a 4-PAM system utilizing an encoding scheme as shown in Figure 2 and having a 800 mV total voltage swing. In this case, the difference between logic levels is approximately 266 mV and the voltage difference between the logic levels and the closest reference voltage is approximately 133 mV. For a system that is using seven bits for the current control signal (CC<6:0>), i.e. N = 7, the LSB(V) is 800 mV/127, or 6.3 mV.

A typical spread for a CMOS process results in a 2.5:1, or even a 3:1, variation in the output driver current from the fast to slow process corners. The term process corner, as used herein, refers to an N-dimensional space where each axis represents a range of values for some process parameter: e.g. threshold voltage, mobility, oxide thickness, etc. A wafer with nominal parameters would represent a point in the center of this N-dimensional space, while a wafer with a combination of anomalous (large deviation from average) parameters would be a point in the corner of this space. Process corners are readily visualized in 2D and 3D space.

The spread in process characteristics is of concern in multi-PAM systems. For example, using the 2.5:1 ratio, the LSB(V) for the fast extreme of the system in the preceding example would be 2.5 * 6.3 mV, or 15.75 mV. Using a current control loop that has an inherent dither, the magnitude of the dither may be as much as +/- LSB(V), or 31.5 mV peak-to-peak. This value is more than 10% of the 266 mV separation between logic levels.

The preferred embodiments therefore provide a way to control the dither under various PVT conditions, such that, in the foregoing example, the dither may be as low as +/- 6.3 mV under all PVT conditions. A further advantage of the preferred embodiments is increased yield. Specifically, the ability to control the dither under all PVT conditions may allow circuits to be used that would otherwise be characterized as unacceptably fast or slow.

Referring now to Figure 18, a first preferred embodiment of a PVT detector 2020 is shown. The PVT detector 2020 includes an input current mirror 2030 that is coupled to an array of NMOS current sources 2040 and an array of PMOS current sources 2050. Each of the current sources 2040 and 2050 drives current into a predetermined load 2060, which for example may be a MOS resistor of a predetermined size. The current sources 2040 and 2050 are preferably weighted, such as by scaling the width or the width-to length ratio of the transistors, to drive correspondingly weighted current values into the loads 2060. An output 2070, representing the voltage drop across the load, is provided.

The PVT detector 2020 of Figure 18 operates as follows. A current, which is independent of PVT conditions, is applied to the input current mirror 2030 at, for example, pin 2080. The PVT independent current may for example be generated from a

bandgap reference (not shown), which is a device that is well known to those skilled in the art. The current is mirrored by the current mirror 2030 to the current sources 2040 and 2050, which in response drive current into the respective loads 2060. The loads 2060 are responsive to PVT conditions. That is, the corresponding resistive value of the MOS resistors shown in Figure 22 will vary in accordance with the PVT conditions. Each of the loads 2060 provides a corresponding output 2070.

The outputs 2070 are preferably coupled to a logic circuit 2090. The logic circuit 2090 decodes the outputs 2070 to determine whether the circuit is "fast," "normal" or "slow." For example, if the PVT conditions are fast, the resistive value of the MOS resistor loads 2060 will be low and all of the outputs 2070 will be small. As a further example, if the PVT conditions are slow, then the resistive value of the loads 2060, and the corresponding outputs 2070, will be high. As described above, the conductance of the FETs may vary over a 2.5:1 ~ 3:1 range . For a nearly constant current as provided by the bandgap reference, the voltage drop across any of the three legs will vary by the same range (i.e. approximately 2.5:1 ~ 3:1). A thermometer code may be used, for example, to decode the outputs 2070. For a fast process, the voltage drop across all the loads 2060 may be low and hence detected as logic low. For a slow process, one or more of the voltage drops across the loads 2060 may be higher and therefore detected as logic high. The logic circuit 2090 therefore senses the PVT conditions based on the outputs 2070 and provides a corresponding current control signal—for example, setting the control signals S1 and S2 in accordance with the state of the outputs 2070.

Figure 19A is a schematic diagram of a second preferred embodiment of a PVT detector 2020. The PVT detector 2020 includes a delay line 2100 followed by a series of

delay stages 2110. An output of each delay stage 2110 is coupled by a latch 2120 to a decoder 2130.

In operation, the latches 2120 are initially cleared by a reset signal. A fire signal, preferably a pulse having a predetermined duration, is generated. For example, the fire signal may have a duration of 2.5 clock cycles, which for a 400 MHz Rambus system, corresponds to approximately 6.25nsec. The signals are preferably full swing CMOS, although other implementations and pulse durations may alternatively be used. The fire signal is preferably derived from, for example, an external clock, so that its duration is PVT insensitive.

The fire signal is applied to the delay line 2100 and the latches 2120, as shown in Figure 19A. When the fire signal is high, the latches are open and any change in the input signal (i1, i2, ... iN) at the "D" side of the latch, such as may be produced as the fire signal propagates through the delay line 2100 and delay stages 2110, produces a corresponding change in the latch output signal (o1, o2, ... oN) at the "Q" side of the latch. On the other hand, when the fire signal is low, the latch output signal is unresponsive to changes in the latch input signal.

In accordance with a first embodiment, N=10. More or fewer delay stages 2110 may, however, alternatively be used.

Figures 19B and 19C are timing diagrams depicting the state of several signals shown in Figure 19A for "slow" conditions and "fast" conditions, respectively. In particular, when the conditions are slow, the delay of the fire signal through the delay line 2100 and the delay stages 2110 causes only one or a few of the latch input signals, such as i1 and i2, to arrive at the corresponding latch 2120 while the fire signal is high. As a

result, most of the latch output signals (o1, o2, ... oN) remain low, and the decoder 2130 determines, based on the state of the latch output signals (o1, o2, ... oN), that the conditions are slow.

When, on the other hand, the conditions are fast, the time delay of the fire signal through the delay line 2100 and the delay stages 2110 is reduced such that most or all of the latch input signals (i1, i2, ... iN) go high within the duration of the fire pulse applied to the latches 2120, as illustrated in Figure 19C. As a result, the corresponding latch output signals (o1, o2, ... oN) switch state, and the decoder 2130 determines, based on the state of the latch output signals, that the conditions are fast.

Figure 20A is an electrical schematic of an embodiment of the PVT detector shown in Figure 19A. A trigger circuit 2140 is coupled to a delay circuit 2150 and a code generating circuit 2160. The output of the code generating circuit is coupled to a decoder circuit 2170. The trigger circuit 2140 generates the fire signal and the reset signal. The delay circuit 2150 produces a delayed version of the fire signal for application to the code generating circuit 2160.

Figure 20B is an electrical schematic of an embodiment of the trigger circuit 2140 shown in Figure 20A. The trigger circuit 2140 receives a set/reset control signal 2180 and a clock signal 2190 and in response generates a fire signal 2200 and a reset signal 2210. In Figure 20B, the SRCTRL signal is pulsed high to begin the current calibration process and flip-flops FF1-FF3 change state on the falling edge of SYNCLK. Signal RESETN remains low for 1 cycle of SYNCLK and clears the state of the latches 2120. Flip-flops FF4-FF6 change on the rising edge of SYNCLK. The FIRE signal is asserted for 2.5 cycles of SYNCLK . The trigger circuit 2140 ensures that there is a pause of 1/2

cycle between the de-assertion of the RESETN, and the assertion of FIRE. Those skilled in the art will recognize, upon reviewing this detailed description, that other implementations of the trigger circuit 2140 may alternatively be used.

Figure 20C is an electrical schematic of an embodiment of the delay circuit 2150 shown in Figure 20A. As shown in Figure 20C, the delay circuit 2150 may be formed from a series of inverters 2220, the outputs of which are capacitively coupled to ground. In accordance with a preferred embodiment, the inverters 2220 are MOS inverters and the capacitors are likewise MOS devices. However, other delay structures, which are known to those skilled in the art, may alternatively be used. The delay circuit 2150 may also include a tuning structure 2155 for tuning the total delay of the delay chain 2150.

Figure 20D is an electrical schematic of an embodiment of the code generating circuit 2160 shown in Figure 20A. Like Figure 19A, Figure 20D includes a series of delay stages 2230 and a corresponding set of latches 2240. An output 2250 is provided by each one of the delay stages 2230 and coupled to a corresponding one of the latches 2240. For example, the first delay stage 2230-1 provides an output, i1, which is coupled to the first latch 2240-1. The latches 2240 receive the fire signal 2200, as a clock input, and the reset signal 2210 from the trigger circuit 2140. The outputs of the latches 2240 are coupled to two outputs 2250, which are provided as inputs to the decoder circuit 2170. In the embodiment of Figure 20D, only 2 latch outputs, 2240-2 and 2240-8, are inspected by the decoder circuit of Figure 20E.

Other implementations of the code generating circuit 2160 may alternatively be used. In addition, more than two latch outputs may be provided to the decoder circuit 2170.

Figure 20E is an electrical schematic of an embodiment of the decoder circuit 2170 shown in Figure 20A. In Figure 20E, the inputs, tap0n and tap1n, are provided by the latch outputs 2240-2 and 2240-8, as shown in Figure 20D. The decoder circuit may decode the latch outputs, 2240-2 and 2240-8, as follows. If both 2240-2 and 2240-8 have not fired, then the process is "slow." If both 2240-2 and 2240-8 have fired, then the process "fast." Otherwise the process is "normal." The logic is resynchronized by the trailing two latches I13-14. In addition, the decoder circuit 2170 may allow the user to override the results of the PVT detector using the "usr" inputs. The outputs SRC1P, SRC0N, etc. may be used to control S1 and S2, as in figure 16, or alternatively to modulate the DACs 2310 or 2320 in Figs 22 and 23 below. Although one embodiment of a decoder circuit is described above, numerous alternatives may be implemented by those skilled in the art upon reading this detailed description.

In systems that include a phase-locked loop (PLL) or a delay-locked loop (DLL), the PLL or DLL may also be used as a PVT detector, rather than using one of the PVT detector embodiments described above. In particular, the PVT conditions may be derived from the state of the loop. For example, when the conditions are "slow," the loop will drive the controlled oscillator or delay line to a high speed condition relative to its normal setting. Conversely, if the conditions are "fast," the loop will slow down the oscillator or the delay stage relative to its normal setting. For a delay-locked loop, the loop logic would merely be decoded to provide a measure of the PVT conditions.

Upon reviewing the foregoing, those skilled in the art may discern other types of PVT detectors that may be suitable for the application described herein. The present invention is not intended to be limited to using the PVT detector embodiments described

above or any particular type of PVT detector. Rather, certain of the preferred embodiments envision the use of a PVT detector, regardless of its implementation particulars, to improve the resolution of a current mode driver.

In accordance with another preferred embodiment of the present invention, a circuit is provided for varying the gate voltage associated with a current mode driver to thereby control the driver's output current, Iout. This provides an additional degree of freedom in the output current adjustment. The current control bits add or remove segments from the driver. The ability to also adjust Vgate allows one to set the minimum output voltage and the output impedance, as well as the current. The inverters that set the current control bits would have their 'on' voltage set by Vgate.

Figure 21A is a schematic diagram of a circuit for controlling an output voltage, Vout. The circuit includes an inverter 2260 having an input 2270, an output 2280 and a control input, Vg. The control input, Vg, is provided by a DAC 2290 through a buffer 2300. The DAC 2290 is controlled by an N-bit control signal.

Figure 21B illustrates for the inverter 2260 the relationship between the input voltage, Vin, and the output voltage, Vout, as a function of the control input, Vg. As shown in Figure 21B, the control input, Vg, limits the output swing of the inverter 2260 and is itself controlled by the DAC 2290.

Figure 22 is an electrical schematic of a first embodiment of the DAC 2290. The DAC 2290 includes a variable current source 2310 that is coupled to ground by a MOSFET 2320. A buffer 2330 is coupled to the gate of the MOSFET 2320. The voltage, Vg, at the gate of the MOSFET 2320 may be controlled by either modulating the current source 2310or adjusting the width-to-length ratio of the MOSFET.

Figure 23 is an electrical schematic of a second embodiment of the DAC 2290. The second embodiment is similar to the embodiment shown in Figure 22, except that the second embodiment includes an additional MOSFET 2340 coupled between the MOSFET 2320 and ground. In this embodiment, the transistors 2320 and 2340 are preferably scaled to match the output driver. That is, the transistors 2320 and 2340 have the same width-to-length ratio, for the same current. Alternatively, if the current were halved in the DAC 2290 to save power, then the width to length ratio is also halved.

The first embodiment of the DAC 2290, shown in Figure 22, and the second embodiment of the DAC 2290, shown in Figure 23, include a variable current source 2310 of which may be used to adjust the gate voltage, Vg. The current source 2310 may be adjusted in accordance with the PVT conditions, such as by utilizing an output of a PVT detector described above. Alternatively, the current source 2310 may be adjusted in accordance with an n-bit current control signal derived, for example, from the calibration process described above with reference to Figures 10, 11A and 11B. As a further alternative, the current source 2310 may be adjusted in accordance with an n-bit current control signal under user control.

Figures 24A and 24B illustrate an electrical schematic of a preferred DAC 2290 and a simulated output of the DAC 2290, respectively. As shown in Figure 24A, an output voltage, VgRef, is adjusted in accordance with an n-bit current control signal, which in this example is up to five bits, Vg_adj <4:0>. The current control bits, Vg_adj <0> through Vg_adj <4> are applied to a corresponding gate of a CMOS transistor, with the transistor width-to-length ratios being scaled as shown in Figure 23A. Those skilled in the art will recognize that more or fewer parallel transistors may be used in alternative

DAC embodiments, although the resolution of the output voltage adjustment is increased as the number of transistors utilized increases.

In Figure 24B, the gate voltage, VgRef, is plotted as a function of time under two operating conditions. For the first set of conditions, represented by the solid line, all five bits of Vg_adj <4:0> are used, with each five-bit control signal from 11111 to 00000 being applied for 1μs. For the second set of conditions, represented by the dashed line, only the two most significant bits of the five bit Vg_adj <4:0> are utilized, with each of the states, 11000, 10000, 01000 and 00000 lasting for 8μs.

As noted above, the current source 2310 in the DAC 2290 may, in accordance with one embodiment of the invention, be adjusted in accordance with the PVT conditions. For this embodiment, a PVT detector, such as one of the PVT detector embodiments described above, provide an output indicative of the PVT conditions. For example, the PVT detector may indicate that the conditions are "fast," "normal" or "slow" by providing a two-bit output signal. This output signal may then be coupled to the DAC 2290 to adjust the output voltage, Vg. In accordance with an example described above with reference to Figure 24B, the two bit output of the PVT detector may be used to control the state of the two most significant bits of the five bit Vg_adj <4:0> current control signal.

As also noted above, however, the DAC 2290 may alternatively be adjusted without regard to the PVT conditions. For example, the current control signals, Vg_adj, <N:0>, may be set by a register during current control calibration as follows. The output voltage, VgRef, is set to a minimum value by applying the appropriate current control signal, Vg_adj <N:0>. Next, as described above with reference to Figures 10, 11A and

11B, the current control calibration circuit determines the settings for the current control bits CC. If the calibration is successful, then a preferred method continues to calibrate the settings for the current control bits CCB and CCC. On the other hand, if the calibration is unsuccessful, for example due to no transition detected at the current control comparator (i.e. (Vhi-Vlo/2) > Vref), then increment Vg_adj <N:0> and repeat the calibration process for CC. The value of Vg_adj <N:0> may continue to be incremented until the calibration of CC is successful.

Upon reviewing the foregoing, those skilled in the art may discern other types of DACs that may be suitable for the application described herein. The present invention is not intended to be limited to using the DAC embodiments described above or any particular type of DAC. Rather, certain preferred embodiments envision the use of a DAC, regardless of its implementation particulars, to improve the resolution of a current mode driver.

In Figure 12, a 4-PAM reference voltage generator 1380 generates the multi-PAM reference voltages VREFHI, VREFM and VREFLO from external voltages, VTERM and VREF, supplied on input pins 1382, 1384 respectively. Unity gain amplifiers 1386, 1388 receive and output the input voltages VTERM and VREF respectively. A voltage divider, including series-connected resistors R1, R2 and R3, is coupled between the outputs of the unity gain amplifiers 1386 and 1388. The lowest voltage VREF is selected to drive V_{REFLO} via a power driver 1390. Power drivers 1392, 1394 are coupled between resistors R3, R2 and R2 to provide reference voltages VREFHI and VREFM respectively. The power drivers 1390-1394 are connected as unity gain amplifiers.

In one embodiment, the resistor values are selected such that resistors R2 and R3 have twice the resistance of resistor R1, and VREF, which is supplied externally, is equal to the desired VREFLO voltage.

An electrical schematic of a first preferred alternative to the current control calibration circuit of Figure 10 is shown in Figures 13A and 13B. In Figure 13A, a comparator 1500 is coupled by a multiplexor 1502 to a multi-level voltage reference 1504, which in this case includes three discrete levels. One of the three reference voltage levels, v_{REFHI}, v_{REFM} or v_{REFLO}, is selectively applied to two inputs of the comparator 1500, as further described below. The comparator 1500 is also coupled to receive source calibration signals 1506 and 1508, which are supplied by current mode drivers, such as the 4-PAM driver 1000 shown in Figure 5A. The source calibration signals 1506 and 1508, for the embodiment shown, include a first driver output at a known, or previously calibrated, voltage level on the input line 1506 and an unknown driver output voltage level on the input line 1508, such that the signal on input line 1508 is the signal being calibrated. The comparator 1500 provides an output for adjusting or calibrating the output of the drivers on input line 1508, as further described below, so that the driver output can be reliably received and decoded.

Figure 13B is an electrical schematic of the comparator 1500 shown in Figure 13A. The two inputs from the multiplexor 1502 and the source calibration signals 1506 and 1508 are each coupled to an input of a switch 1510. The outputs of the switches 1510 are combined in pairs and each combined switch output is connected to a coupling capacitor 1512. The coupling capacitors 1512 are connected to opposing inputs 1514a and 1514b of a transistor comparator 1516. The output of the transistor comparator 1516

is the voltage across nodes 1518 and 1520. Two switches 1522 selectively couple the output nodes 1518 and 1520 to the inputs 1514a and 1514b, respectively. The output nodes 1518 and 1520 are coupled to a latching stage 1524.

As illustrated in Figure 13B, the elements of the comparator 1500, including the switches 1510, the coupling capacitors 1512, the amplifier 1516 and the switches 1522, are preferably implemented as semiconductor devices in an integrated circuit. The coupling capacitors 1512 are preferably constructed using MOS transistors connected as capacitors but other embodiments may alternatively use other capacitor types. Those skilled in the art of integrated circuit design will appreciate that, as a result of process variation, there is likely to be a random offset voltage associated with the transistor comparator 1516. In other words, if the same voltage is applied at the inputs 1514a and 1514b, a finite voltage will appear across output nodes 1518 and 1520, rather than the ideal case in which the output nodes 1518 and 1520 are at the same potential. While the offset voltage is not typically significant for systems using binary or 2-PAM signaling, it is preferable to correct for the offset voltage in systems using four or more signal levels, such as a 4-PAM system.

The comparator 1500 of Figure 13B therefore includes offset cancellation circuitry. Specifically, the coupling capacitors 1512 and the switches 1522 are operable to provide offset cancellation as follows. During the cancellation phase, which may also be referred to herein as the auto-zero phase, signal az, which is coupled to the gates of the transistor switches 1522, is high. Referring back to Figure 13A momentarily, the signal az is generated by a non-overlapping clock driver, which includes elements U29, U16,

U18, etc. The non-overlapping clock driver produces skewed signals, with a delay period between transitions.

Referring again to Figure 13B, when the signal az goes high, the amplifier 1516 is placed into unity gain mode by turning on switches 1522 and the offset voltage is stored on the coupling capacitors 1512. In addition, during the auto-zero phase, the switches 1510 are set to apply, in this particular embodiment, the reference voltage supplied by the multiplexor 1502 and the known output driver voltage 1506 to the coupling capacitors 1512. Thus, during the auto-zero phase, the transistor comparator 1516 samples the difference between the two known voltages as modified by the offset voltage of transistor comparator 1516.

At the end of the auto-zero phase, switches 1522 are opened, placing the amplifier 1516 into a high gain mode, and then there is a momentary delay followed by a compare phase. At the start of the compare phase, the state of the switches 1510 is changed to sample the reference voltage supplied by the multiplexor 1502 and the unknown output driver voltage 1508 onto the coupling capacitors 1512. Because the charge stored from the auto-zero phase is trapped on the coupling capacitors 1512, any change in the input voltages, such as the change to the unknown output driver voltage 1508, produces a voltage across the input nodes 1514a and 1514b of the transistor comparator 1516. This in turn produces an output voltage across the nodes 1518 and 1520 that is preferably latched into the latching stage 1524.

The control logic enables strobing of the latching stage 1524. In accordance with a preferred embodiment, the latch 1524 may be strobed multiple times during a single

compare phase. Alternatively, the latch 1524 may be strobed only once during a single compare phase.

In accordance with a preferred embodiment, a current control transistor in the current mode driver is adjusted, for example as described above with respect to Figures 10, 11A and 11B or as described in U.S. Patent No. 5,254,883, based upon the output of the transistor comparator 1516. In accordance with a preferred embodiment, the unknown driver output voltage level on line 1508 is incrementally adjusted, such as by increasing or decreasing the amount of current sunk by the output driver, until the average value of the voltage levels on lines 1506 and 1508 is equal to the reference voltage supplied by the multiplexor 1502.

Figure 13C is a timing diagram illustrating the relationship between several of the signals referenced above. The timing signals 1526 and 1528 drive the non-overlapping clock driver in Figure 13A. The auto-zero and compare phases are defined in accordance with the signal 1526. The signal 1530 is the voltage output of the comparator, as shown at pin 1532 in Figure 13A. The known voltage signal 1506 and the known voltage reference from the multiplexor 1502 are essentially constant. The unknown voltage signal 1508 is adjusted, in this example it is decreasing. When the unknown voltage signal 1508 reaches the point where the reference voltage is equal to the average of the signals 1506 and 1508, the output of the comparator circuit 1530 goes high.

The current control calibration circuit shown in Figures 13A and 13B may be utilized as follows to calibrate a 4-PAM output driver, such as the driver of Figure 5A. When the transistors 1002, 1004 and 1006 are in the "off" state the voltage at the output

of the current mode driver is v_{TERM}. This corresponds to the symbol 00, which is the zero current state and does not need to be calibrated.

The known voltage, v_{TERM}, is applied to line 1506 of the comparator 1500 and an unknown voltage generated by turning "on" the transistor 1002 (from Figure 5A) is applied to line 1508 of the comparator 1500. The multiplexor 1502 causes the reference voltage, v_{REFHI}, to be applied to the comparator 1500. Using feedback from the output of the comparator 1500, a current control transistor (not shown) coupled in series with the transistor 1002 is adjusted until the average of the voltages on lines 1506 and 1508 is equal to the reference voltage, v_{REFHI}. The voltage on line 1508 is now calibrated to correspond with the 4-PAM symbol "01".

At this point, the voltage corresponding to the 4-PAM symbol "01" is applied to line 1506, and an unknown voltage generated by turning "on" the transistors 1002 and 1004 is applied to line 1508. The multiplexor 1502 is activated to cause the reference voltage, v_{REFM}, to be applied to the comparator 1500. Using feedback from the output of the comparator 1500, a current control transistor (not shown) coupled in series with the transistor 1004 is adjusted until the average of the voltages on lines 1506 and 1508 is equal to the reference voltage, v_{REFM}. The voltage on line 1508 is now calibrated to correspond with the 4-PAM symbol "11".

Next, the voltage corresponding to the 4-PAM symbol "11" is applied to line 1506, and an unknown voltage generated by turning "on" the transistors 1002, 1004 and 1006 is applied to line 1508. The multiplexor 1502 is activated to cause the reference voltage, v_{REFLO}, to be applied to the comparator 1500. Using feedback from the output of the comparator 1500, a current control transistor (not shown) coupled in series with the

transistor 1006 is adjusted until the average of the voltages on lines 1506 and 1508 is equal to the reference voltage, v_{REFlo}. The voltage on line 1508 is now calibrated to correspond with the 4-PAM symbol "10".

Those skilled in the art of circuit design will appreciate that the comparator 1500 may take other forms. Figure 13D illustrates alternative embodiments for the differential comparator of Figure 13B.

Referring again to Figure 13B, it will be appreciated that if, for example, the comparator 1500 is implemented as an integrated circuit, then the coupling capacitors 1512 may be implemented using a PMOS FET topology as shown in Figure 13E. Such capacitors operate linearly when the applied voltage, v_{DC}, is greater than the magnitude of the threshold voltage, v_T, of the PMOS FET. The averaging and offset cancellation functions of the comparator 1500 are not optimally realized when the capacitors are operated in the non-linear range. It is therefore preferred that the applied voltage be kept within the linear range. In accordance with a preferred embodiment, the applied voltage is within the range of approximately 1.0 volts to 1.8 volts. The auto-zero voltage, v_{AZ}, may be approximately 0.6 volts.

An electrical schematic of another preferred alternative to the current control calibration circuit of Figure 10 is shown in Figures 14A and 14B. As shown in Figure 14A, this embodiment includes a comparator 1500, a multiplexor 1502, multi-level voltage reference 1504, and source calibration signals 1506 and 1508, which carry a known voltage signal and an unknown (to be calibrated) voltage signal, respectively. In comparison to Figure 13A, the circuit of Figure 14A differs in that it includes a resistive voltage combiner 1532 that is coupled to provide the average of the signals on lines 1506

and 1508 to the comparator 1500. In addition, for the embodiment of Figure 14A, the non-overlapping clock driver is replaced by an inverter delay chain 1534.

As shown in Figure 14B, the comparator 1500 differs from that of Figure 13B. Notably, a different offset cancellation technique is utilized. For the embodiment of Figure 14B, a switch 1536 and feedback amplifier 1538 are used to compensate for the offset voltage associated with a differential amplifier 1540.

The operation of the embodiment shown in Figures 14A and 14B will now be described. The timing of the offset cancellation phase and the compare phase are controlled by the inverter delay chain 1534. The inverter delay chain 1534 produces skewed signals evb, evb2, evb6, etc, shown in Figures 14C and 14D. The delay between these signals is approximately the delay of one or more logic gates. The delay period may be augmented by loading the gate outputs with additional capacitance.

During the cancellation phase, the feedback amplifier 1538 senses the offset voltage associated with the differential amplifier 1540 as follows. When timing signal evb2 goes low, the inputs 1542 and 1544 of the amplifier 1540 are shorted together by a switch 1546. At the same time, a switch pair 1548 couples the outputs of the amplifier 1540 to the inputs of the feedback amplifier 1538. With the inputs 1542 and 1544 of the amplifier 1540 being shorted together, any voltage appearing at the output of the amplifier 1540 may be characterized as an output offset voltage. The feedback amplifier 1538 produces output current in the drains of transistors 1550 and 1552 in an amount that is proportional to the output offset voltage. The current supplied by the feedback amplifier 1538 works to drive the output offset voltage to zero, thereby balancing the amplifier 1540 when its inputs 1542 and 1544 are shorted. The resultant voltage required

to produce the balancing current in the feedbac amplifier 1538 is stored on the capacitors 1554 and 1556 at the end of the cancellation phase when the switches 1548 are opened.

As shown in Figures 14C and 14D, shortly after the cancellation phase ends on the falling edge of the signal evb, the switches 1546 and 1548 are opened, disconnecting the feedback amplifier 1538 and coupling the inputs 1542 and 1544 to the amplifier 1540, as the signal evb2 goes high. The transition of evb2 to high starts the compare phase. Momentarily after the compare phase starts, the signal evb6 goes high, activating the latching stage of the comparator 1500. When the latching stage is active, the output voltage of the differential amplifier 1540 is latched.

The current control calibration circuit shown in Figures 14A and 14B may be utilized to calibrate a 4-PAM output driver in the same manner as described above with respect to Figures 13A and 13B.

Figure 15A is an electrical schematic of a linear transconductor. In a linear region of operation, the output voltage, v_{OUT}, is proportional to the difference between the input voltages, v_1 and v_2. Thus, the output of the linear transconductor is balanced, i.e. $v_{OUT}= 0$, when $v_1 - v_{Ref} = v_{Ref} - v_2$, or $(v_1 + v_2)/2 = v_{Ref}$.

In accordance with yet another alternative embodiment, therefore, the comparator comprises a transconductor stage, as shown in Figure 15B. For this embodiment, an offset canceling amplifier, such as the amplifier 1538 of Figure 14B, is preferably utilized.

While the invention has been described in connection with a number of preferred embodiments, the foregoing is not intended to limit the scope of the invention to a particular form, circuit arrangement, or semiconductor topology. To the contrary, the

invention is intended to be defined by the appended claims and to include such alternatives, modifications and variations as may be apparent to those skilled in the art upon reading the foregoing detailed description.